

What is claimed is:

1 1. A method of controlling the top width of a deep
2 trench, comprising the steps of:
3 providing a substrate having a trench therein;
4 forming a first conductive layer and filling a portion
5 of the trench;
6 forming a α -silicon layer on the sidewall of the trench
7 and the first conductive layer, wherein the α -
8 silicon is thicker at the top of the trench than
9 elsewhere;
10 oxidizing the α -silicon layer to form a silicon oxide
11 layer;
12 forming a dielectric layer on the silicon oxide layer,
13 and anisotropically etching the dielectric layer
14 and the silicon oxide layer to form a collar
15 dielectric layer on the sidewalls of the trench;
16 forming a second conductive layer to fill the trench,
17 with a lower surface than the trench; and
18 recessing the collar dielectric layer below the second
19 conductive layer such that the substrate surface
20 at the sidewall of the trench is exposed.

1 2. The method of controlling the top width of a deep
2 trench as claimed in claim 1, wherein the substrate is a
3 single crystal silicon substrate.

1 3. The method of controlling the top width of a deep
2 trench as claimed in claim 1, formation of the first
3 conductive layer further comprising:

4 depositing the conductive layer on the substrate and
5 filling into the trench; and
6 etching back the conductive layer to form a recess in
7 the trench.

1 4. The method of controlling the top width of a deep
2 trench as claimed in claim 3, wherein the conductive layer
3 is formed by chemical vapor deposition.

1 5. The method of controlling the top width of a deep
2 trench as claimed in claim 3, wherein the conductive layer
3 is etched by anisotropic dry etching.

1 6. The method of controlling the top width of a deep
2 trench as claimed in claim 1, wherein the first conductive
3 layer is an n⁺-type doped polysilicon.

1 7. The method of controlling the top width of a deep
2 trench as claimed in claim 1, the trench further comprising
3 a capacitor and the conductive layer acting as a top
4 electrode of the capacitor.

1 8. The method of controlling the top width of a deep
2 trench as claimed in claim 1, wherein the α -silicon is
3 thicker at the top than the bottom.

1 9. The method of controlling the top width of a deep
2 trench as claimed in claim 8, wherein the thicker α -silicon
3 at the top of the trench is formed by chemical vapor
4 deposition.

1 10. The method of controlling the top width of a deep
2 trench as claimed in claim 1, the steps of forming the
3 second conductive layer further comprising:

4 depositing the conductive layer on the substrate and
5 filling into the trench; and
6 etching back the conductive layer to form a recess in
7 the trench.

1 11. The method of controlling the top width of a deep
2 trench as claimed in claim 1, wherein the dielectric layer
3 is TEOS oxide.

1 12. The method of controlling the top width of a deep
2 trench as claimed in claim 1, wherein a portion of the
3 silicon oxide and the collar dielectric is removed by wet
4 etching.

1 13. A method of controlling the top width of a deep
2 trench, comprising the steps of:

3 providing a semiconductor silicon substrate having a
4 trench therein, and filling a first polysilicon
5 layer in a portion of the trench;

6 forming a α -silicon layer on the sidewall of the trench
7 and the first conductive layer, with α -silicon at
8 the top of the trench being thicker than
9 elsewhere;

10 oxidizing the α -silicon layer to form a silicon oxide
11 layer;

12 forming a dielectric layer on the silicon oxide layer,
13 and anisotropically etching the dielectric and

14 silicon oxide layer to form a collar dielectric
15 layer on the sidewall of the trench;
16 forming a second conductive layer and filling into the
17 trench, having a lower surface than the trench,
18 and;
19 removing a portion of the collar dielectric layer,
20 forming a surface lower than the second
21 conductive layer.

1 14. The method of controlling the top width of a deep
2 trench as claimed in claim 13, wherein the substrate is a
3 single crystal silicon substrate.

1 15. The method of controlling the top width of a deep
2 trench as claimed in claim 13, formation of the first
3 conductive layer further comprising:
4 depositing the conductive layer on the substrate and
5 filling the trench; and
6 etching back the conductive layer to form a recess in
7 the trench.

1 16. The method of controlling the top width of a deep
2 trench as claimed in claim 15, wherein the first conductive
3 layer is formed by chemical vapor deposition.

1 17. The method of controlling the top width of a deep
2 trench as claimed in claim 13, wherein the first conductive
3 layer is etched by anisotropic dry etching.

1 18. The method of controlling the top width of a deep
2 trench as claimed in claim 13, wherein the first conductive
3 layer is an n⁺-type doped polysilicon.

1 19. The method of controlling the top width of a deep
2 trench as claimed in claim 13, the trench further comprising
3 a capacitor and the conductive layer acting as a top
4 electrode of the capacitor.

1 20. The method of controlling the top width of a deep
2 trench as claimed in claim 13, wherein the α -silicon is
3 thicker at the top than the bottom.

1 21. The method of controlling the top width of a deep
2 trench as claimed in claim 20, wherein the thicker α -silicon
3 is formed by chemical vapor deposition.

1 22. The method of controlling the top width of a deep
2 trench as claimed in claim 13, the steps of forming the
3 second conductive layer further comprising:

4 depositing the conductive layer on the substrate and
5 filling into the trench; and
6 etching the conductive layer to form a recess in the
7 trench.

1 23. The method of controlling the top width of a deep
2 trench as claimed in claim 13, wherein the dielectric layer
3 is TEOS oxide.

1 24. The method of controlling the top width of a deep
2 trench as claimed in claim 13, wherein a portion of the
3 silicon oxide and the collar dielectric is removed by wet
4 etching.